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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,774	12/28/2001	Michael Burrows	9772-0337-999	2125
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MORGAN, LEWIS & BOCKIUS, LLP. 2 PALO ALTO SQUARE 3000 EL CAMINO REAL PALO ALTO, CA 94306			ROMANO, JOHN J	
			ART UNIT	PAPER NUMBER
			2192	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/040,774	Applicant(s) BURROWS ET AL.	
	Examiner John J. Romano	Art Unit 2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 September 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Remarks

Applicants' amendment dated September 14th, 2005, responding to the November 3rd, 2004, Office action provided in the rejection of claims 1-33, wherein claims 1, 2, 12, 13, 23 and 24 have been amended and claims 34-36 have been added. Claims 1-36 remain pending in the application and which have been fully considered by the examiner.

1. Applicant arguing for the claims being patentable over *Chase* (see pages 12-18 of the amendment and response) primarily based on assertions on pages 14-16, and arguments pertaining to the dependent claims are not persuasive, as will be addressed under Prior Art's Arguments – Rejections section at item 2 and the claim rejections below. Accordingly, Applicants' arguments and amendments necessitated additional clarifications and rejections, in light of the rejection of the claims over prior art provided in the previous Office action. Thus, the rejection of the claims over prior art in the previous Office action is maintained in light of the necessitated additional clarifications provided hereon and **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

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extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Prior Art's Arguments – Rejections

2. Applicant's arguments filed September 14th, 2005, in particular on pages 14-16, have been fully considered but they are not persuasive. For example,

(A) In regard to the argument that *Chase* does not teach or suggest a method of dynamically verifying program operation in which a shadow array is maintained while executing a specified computer program, the method including determining whether execution of the instruction is inconsistent with an entry of the shadow array (Page 14, third paragraph of the amendment and response), the Examiner respectfully disagrees. The Applicant asserts that *Chase* does not teach or suggest a shadow array being maintained while executing a computer program. The Applicant then provides as evidence that the *Chase* patent discloses comparing "declarations of programming language entities from separately compiled modules" (Page 15, first paragraph of the amendment and response) and deriving a data type from the context of a code function. While the Examiner agrees that *Chase* indeed teaches link-time error detection, *Chase* in the very next paragraph also teaches run-time error detection (Column 4, lines 50-55), wherein he discloses:

"For **run-time** error detection, the inventive techniques allow for the recovery of the type of a region of memory in languages, such as C and C++,

that do not ordinarily allow programs to recover such information. This **type information allows a run-time checking** implementation to diagnose errors such as RT3 and RT4 (from above).”, (bold for emphasis), wherein the type information is checked dynamically during run-time.

Thus, the fact that *Chase* discloses link-time error detection does not exclude *Chase* from teaching run-time detection. Accordingly, *Chase* does teach the instant features of claim 1.

(B) In regard to Applicant’s next argument, that *Chase* also fails to teach or suggest a shadow array having entries corresponding to respective memory locations used by the specified computer program as recited in claim 1, the Examiner respectfully disagrees. The definition of the RT4 errors diagnosed are disclosed by *Chase* below:

“RT4. Incorrect interpretation of the type of object designated by a pointer. In the case of C or C++, this can happen because the program performed an unintended or illegal type cast operation, or the program accessed a member of a union after a value was stored in a different member of the union, or the program released a **dynamically allocated chunk of memory**, then reallocated that **same memory as a different type**.” (Column 2, lines 30-39).

The dynamically allocated chunk of memory disclosed above, allocated as a different type directly correspond to respective memory locations used by the specified computer program as recited in claim 1. Therefore, the rejection is maintained in light of Applicant’s instant argument.

(C) In regard to Applicants arguments with respect to new claims 34-36. The arguments are moot based on the grounds of rejection provided below in the claim rejections.

(D) In regard to Applicant's arguments with respect to the remaining independent claims, the arguments are not persuasive as addressed above in sections (A) and (B) and below in section (E).

(E) In regard to Applicant's arguments with respect to Page 18, second paragraph of the amendment and response, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Claim Rejections

Claims **1-36** are pending in this action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1 - 6, 8 - 10, 12 - 17, 19 – 21, 23 – 28, 30-32 and 34-36** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Chase et al., US 6,149,318, (hereinafter **Chase**).

In regard to claim **1**, **Chase** discloses:

- *"A method of dynamically verifying program operation, comprising: executing a specified computer program..."* (E.g., see Figure 4 & Column 17, lines 10 – 26), wherein, dynamic or run-time verification of a specific program is achieved via instrumentation.
- *"...while executing the specified computer program, maintaining a shadow array, the shadow array having entries corresponding to respective memory locations used by the specified computer program, each entry of the shadow array indicating a data type of the corresponding respective memory location..."* (E.g., see Figure 4 & Column 18, lines 3 - 7), wherein, the table is the shadow array.
- *"...the execution of the specified computer program including executing each of a plurality of instructions of the computer program, wherein execution of each instruction of a subset of the plurality of instructions includes: determining whether a memory access for executing the instruction is inconsistent with a data type entry of the shadow array and generating a report when an inconsistency is determined; executing the instruction; and updating the shadow array in accordance with execution of the instruction."* (E.g., see Fig 8 & Column 17, lines 10 – 26), wherein, the record of types is maintained, wherein the record may be a table (shadow array), and referenced for consistency or inconsistency, for reporting errors or generating a report. Additionally, as further disclosed (Column 19, lines 59-63),

when local variables information tables are within the routine, the variables active in those scopes and the types are organized into several arrays.

In regard to claim **2**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*identifying a memory location to be accessed by the instruction; inspecting the shadow array entry corresponding to the identified memory location; and determining whether execution of the instruction is inconsistent with the inspected shadow array entry corresponding to the identified memory location.*" (E.g., see Figure 4 & Column 17, lines 10 – 24), wherein, the first data structure maps the location and the second maps the type and returns a Boolean indicating an error or not, wherein the types and bounds are directly associated with memory addresses.

In regard to claim **3**, **Chase** discloses the method of claim **2** as described above and furthermore, **Chase** discloses:

- "...*comprises a read operation...*" (E.g., see Figure 4 & Column 32, lines 38 - 48), wherein, the computer reads the memory.

In regard to claim **4**, **Chase** discloses the method of claim **2** as described above and furthermore, **Chase** discloses:

- "...comprises a write operation..." (E.g., see Figure 4 & Column 32, lines 38 - 48), wherein, the computer writes to memory to operate to perform the function of maintaining the table or shadow array.

In regard to claim **5**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...includes determining whether proper execution of the instruction requires accessing data of a predefined data type that is different from the data type specified by the entry of the shadow array." (E.g., see Figure 4 & Column 17, line 51 – Column 18, line 7), wherein, a data structure would be defined and later queried to see if complete.

In regard to claim **6**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...is inconsistent with the data type specified..." (E.g., see Figure 4 & Column 6, lines 14 – 19), wherein improperly corresponding or inconsistent to the common given program entity or data type specified.

In regard to claim **8**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...indicates whether the corresponding memory location has been allocated." (E.g., see Column 18, line 56 – Column 19, line 5), wherein, the table is registered and manipulated to correspond to allocated memory.

In regard to claim **9**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*has been initialized.*" (E.g., see Column 20, lines 6 – 18), wherein, the table or shadow array is initialized.

In regard to claim **10**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*compiling a source code program into a specified computer program...*" (E.g., see Figure 4 & Column 4, lines 12 – 19), wherein, the language processor or compiler where the front end input is a source code program and the abstract syntax tree or intermediate code is the specified computer program.
- "...obtaining debugging information related to the specified computer program; and initializing the shadow memory based on the debugging information." (E.g., see Figure 18 & Column 13, lines 17 - 20), wherein, information obtained from the intermediate code is used to initialize the table or shadow memory and then validate or debug the program.

In regard to claim **12**, Claim **12** is a product version of claim **1** and thus, the limitations described in claim **1**, respectively correspond to claim **12**. **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*an interpreter module.*" (E.g., see Column 32, lines 36 – 37), wherein, the language may be interpreted.

Claims **13 - 17**, and **19 - 21** are product versions of the method claims of **2 - 6** and **8 - 10**, respectively. Thus, the limitations as described in the corresponding claims apply to and meet the limitations of claims **13 - 17** and **19 - 21**.

In regard to claim **23**, Claim **23** is a product version of claim **1** and thus, the limitations described in claim **1**, respectively correspond to claim **12**. **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...a program instrumenting module for adding dynamic checking instructions to a compiled program to generate an instrumented program..." (E.g., see Column 2, lines 40 - 53), wherein, the program is instrumented for run-time checking or dynamic checking instructions to a compiled program to generate an instrumented program.

Claims **24 - 28** and **30 - 32** are product versions of the method claims of **2 - 6** and **8 - 10**, respectively. Thus, the limitations as described in the corresponding claims apply to and meet the limitations of claims **24 - 28** and **30 - 32**.

In regard to claims **34-35**, the rejections of base claims **1** and **12**, respectively, are incorporated. Furthermore, **Chase** discloses:

- "...performing data-type checking by at least one of instrumenting the specified computer program and by interpreting the plurality of instructions as they are executed without modifying the plurality of instructions..." (E.g., see Column 2, lines 40 - 53), wherein, the added instructions include instrumenting the specified computer program.

In regard to claim **36**, the rejections of base claim **23** is incorporated.

Furthermore, **Chase** discloses:

- "...the dynamic checking instructions include at least one of instrumenting the specified computer program and interpreting the plurality of instructions as they are executed without modifying the plurality of instructions..." (E.g., see Column 2, lines 40 - 53), wherein, the added instructions include instrumenting the specified computer program.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims **7, 18 & 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chase** in further view of Chao et al., US 5,995,752, (hereinafter **Chao**).

In regard to claim **7**, **Chase** discloses the method of claim **1**, as described above and furthermore, **Chase** discloses:

- "... stack locations, and memory heap locations." (E.g., see Figure 4 & Column 18, line 27 – Column 19, line 21), wherein, it is well known in the art that a user-controlled memory location in assembly may be a CPU register.

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But **Chase** does not expressly disclose "... *CPU registers*...". However **Chao** discloses:

- "... *CPU registers*..." (E.g., see Column 3, lines 17 - 22), wherein, the CPU registers are saved in order to keep current memory status.

Chase and **Chao** are analogous art because they are both concerned with the same field of endeavor, namely, memory status operations. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine via assembly language CPU registers with **Chase's** invention of run-time error checking. The motivation to do so would have been to make system specific calls (E.g., see Chase Column 19, lines 13 – 14). Also, **Chase** makes reference to implementing a run-time program in "assembly language" (Column 32, line 35) which would imply using CPU registers.

In regard to claims **18 & 29**, these claims are product versions of claim **7**. Thus, the limitations, as described in the corresponding claim, apply to and meet the limitations of claims **18 & 29**.

5. Claims **11, 22 & 33** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chase** in further view of Grossman et al., US 5,987,249, (hereinafter **Grossman**).

In regard to claim **11**, **Chase** discloses the method of claim **1** as described above. But **Chase** does not expressly disclose "... *not executing the instruction when execution of the instruction is determined to be inconsistent*...". However, **Grossman** discloses:

- "...*not executing the instruction when execution of the instruction is determined to be inconsistent...*", (E.g., see Column 18, lines 47 – 54), wherein, **Grossman** teaches stopping execution of the code in response to an error or inconsistent type.

Chase and Grossman are analogous art because they are both concerned with the same field of endeavor, namely, program instrumentation for run-time error checking. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to stop a program when finding an error in Chase' run-time error checking instrumentation. The motivation to do so would have been to stop a faulty program from running and doing more damage. Thereby, wasting further time and money.

In regard to claims **22 & 33**, claims **22 & 33** are a product version of claim **11**. Thus, the limitations, as described in the corresponding claim, apply to and meet the limitations of claims **22 & 33**.

Conclusion


Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Romano whose telephone number is (571) 272-3872. The examiner can normally be reached on 8-5:30, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJR



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SUPERVISORY PATENT EXAMINER